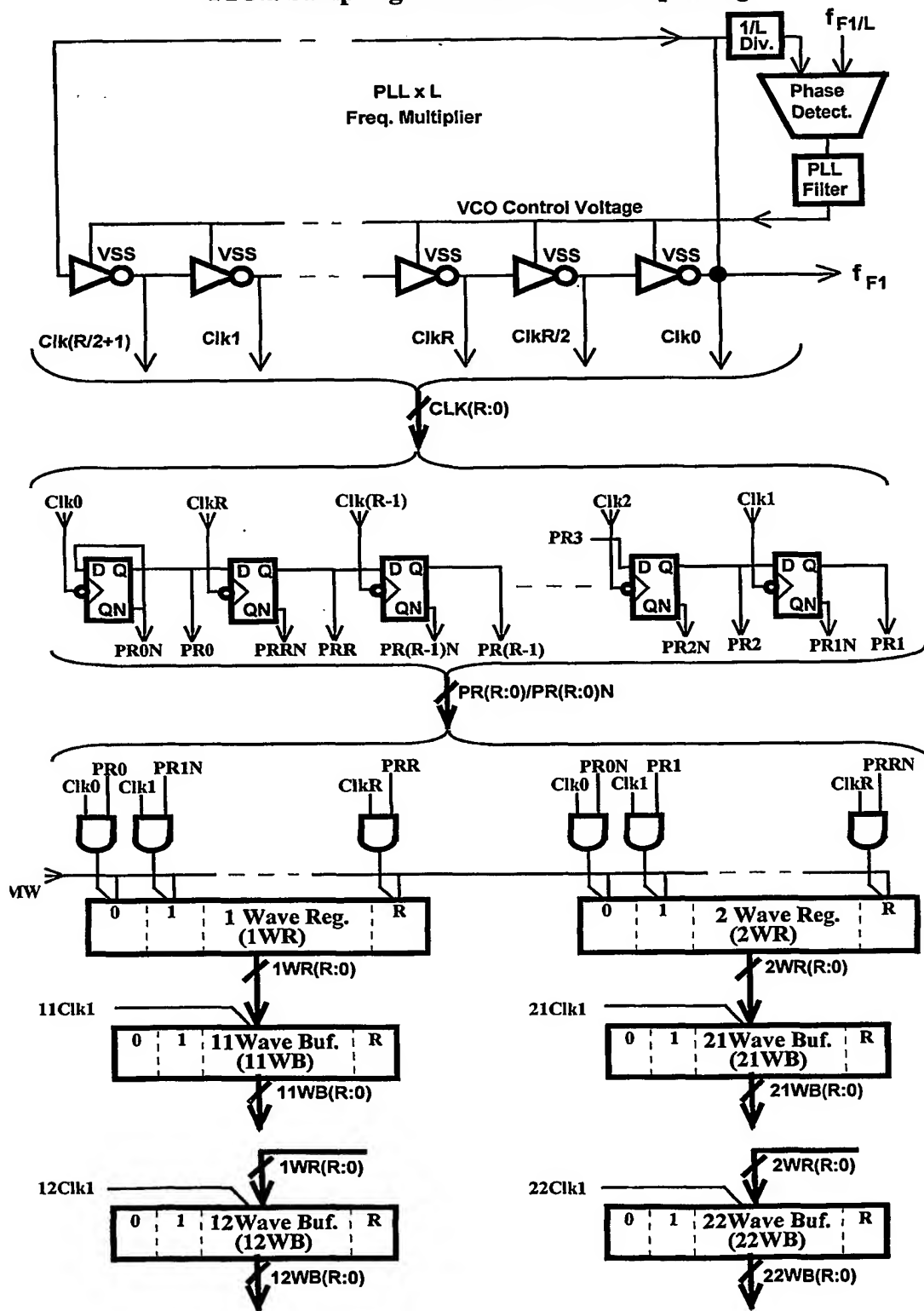


FIG.1 Sampling Clocks and Wave Capturing



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FIG.2A Sequential Clocks Generation (SCG)

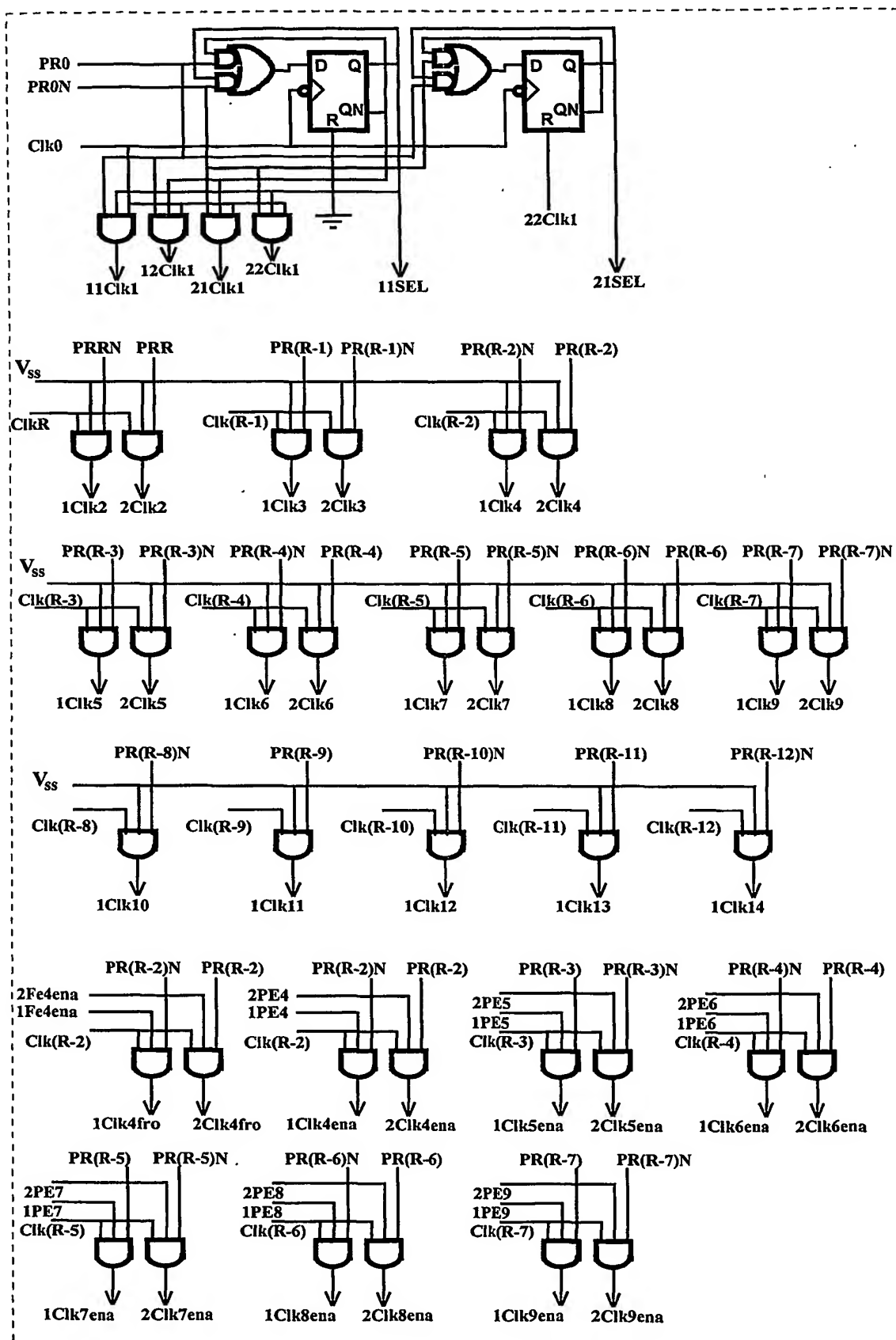


FIG.2B Sequential Phase Control (SPC)

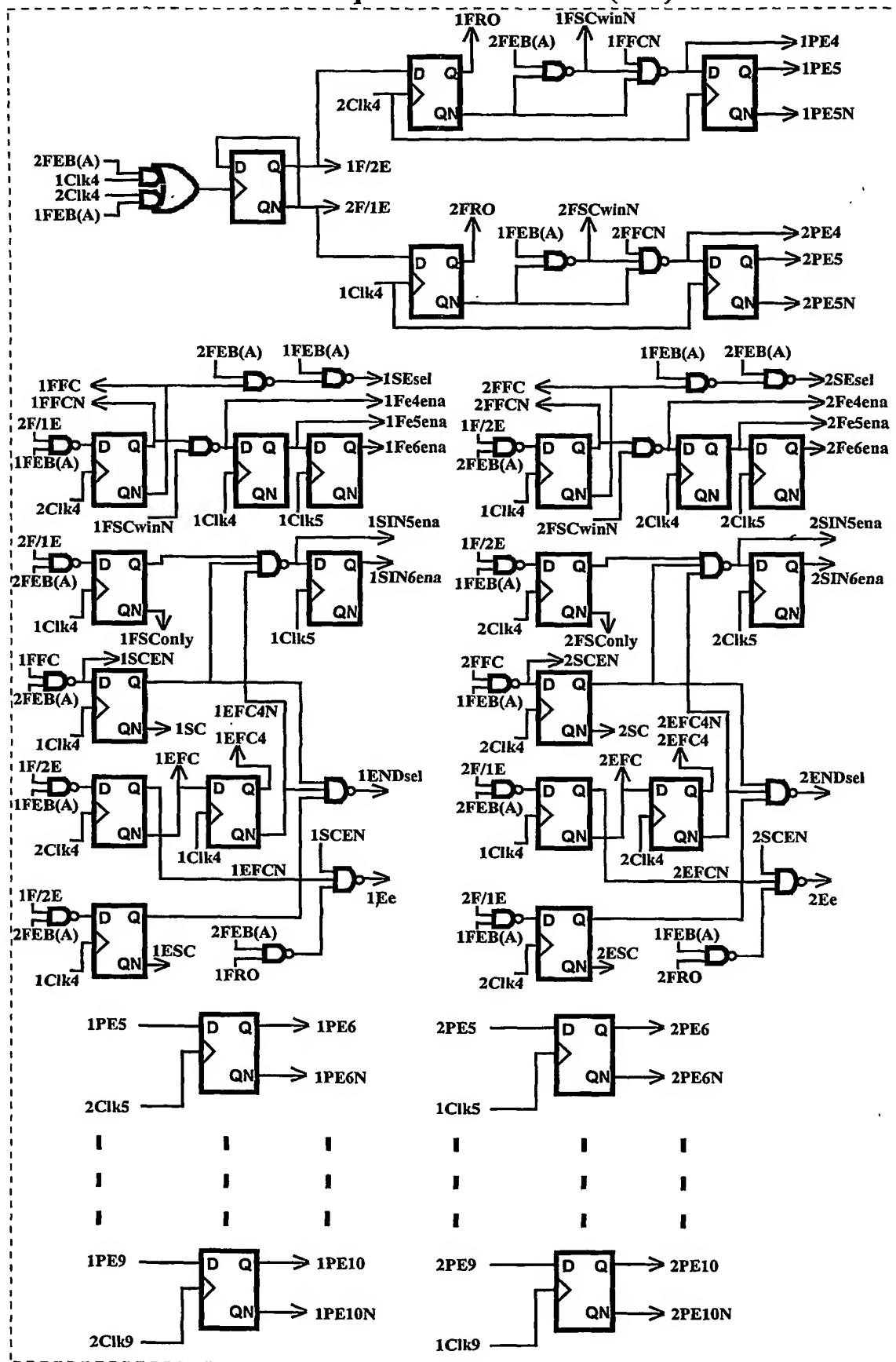
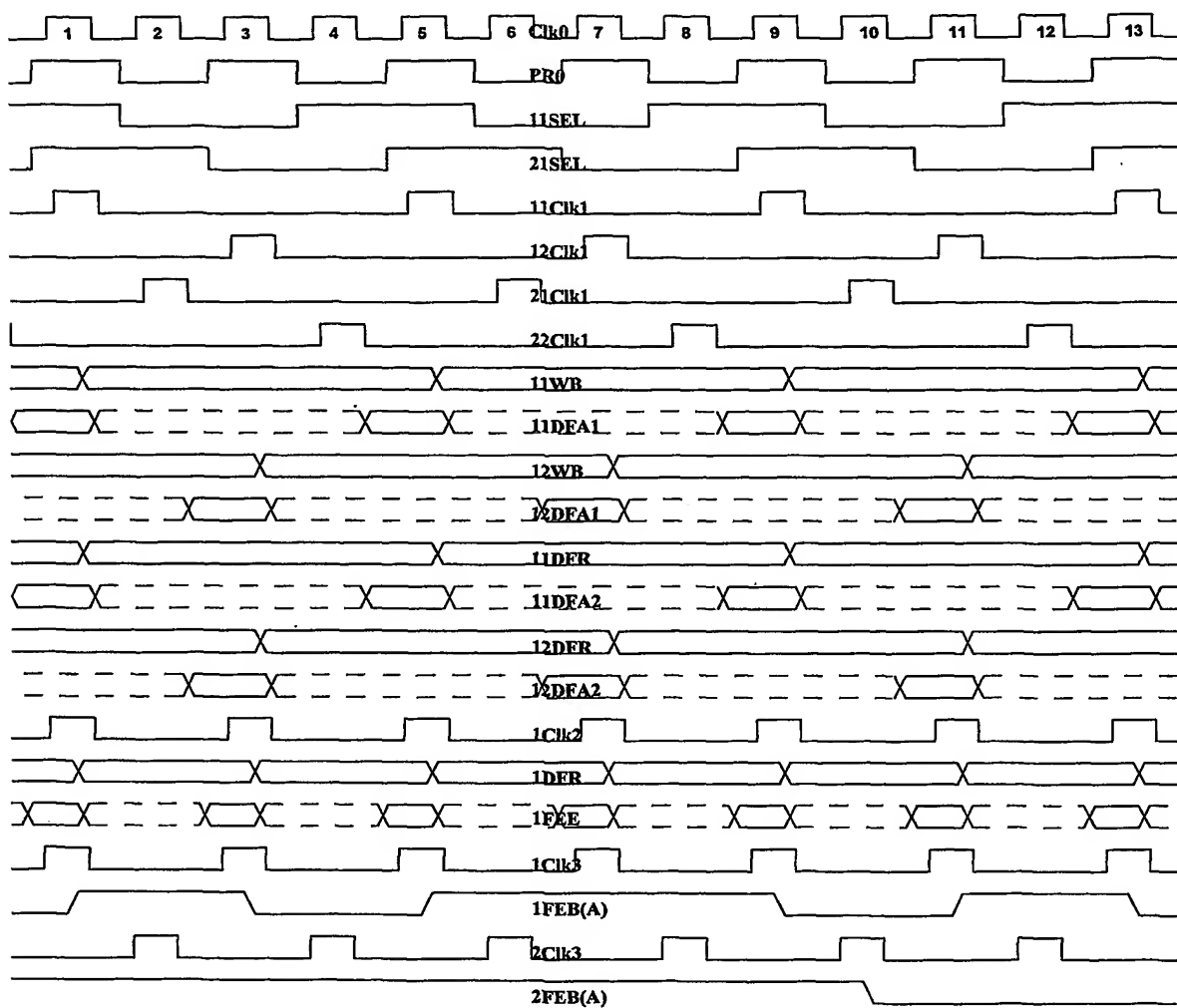


FIG.2C Timing Diagram of the SC and WC

**FIG.2D Timing Diagram of Sequential Phase Control
preceded by a phase2 long data string (continuation of FIG.2C)**

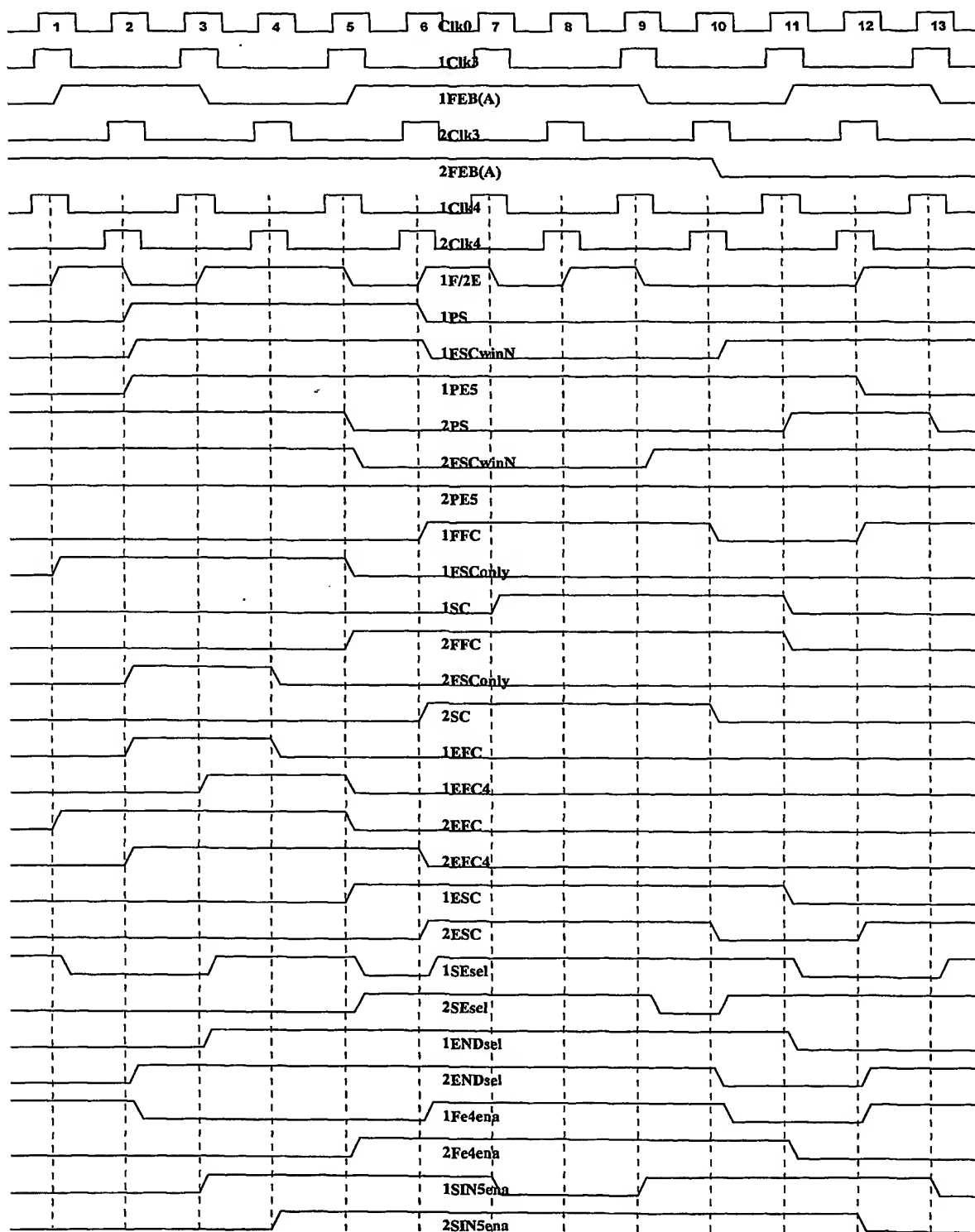


FIG.3A Phase1 of the Phase Processing Stages

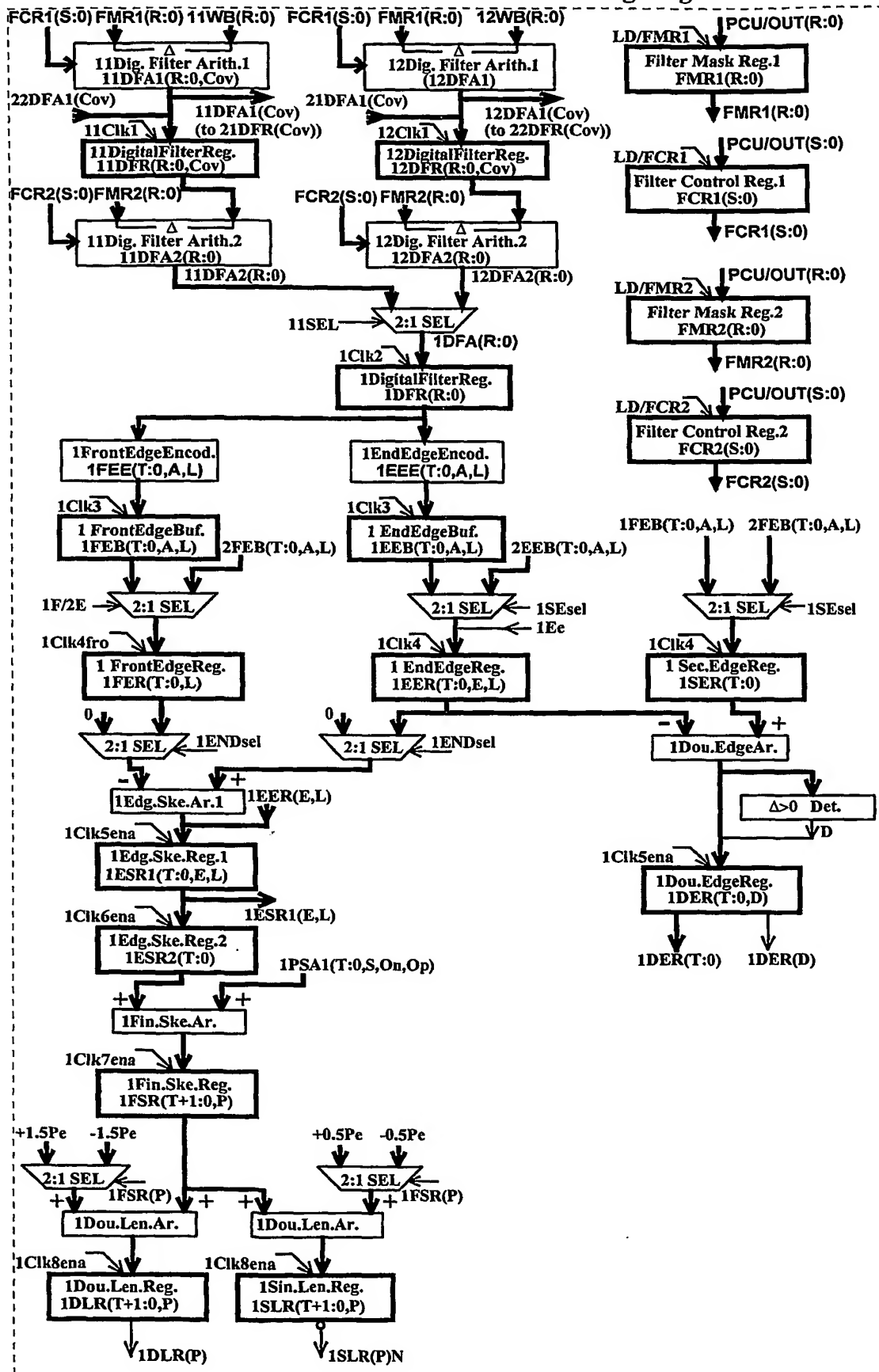
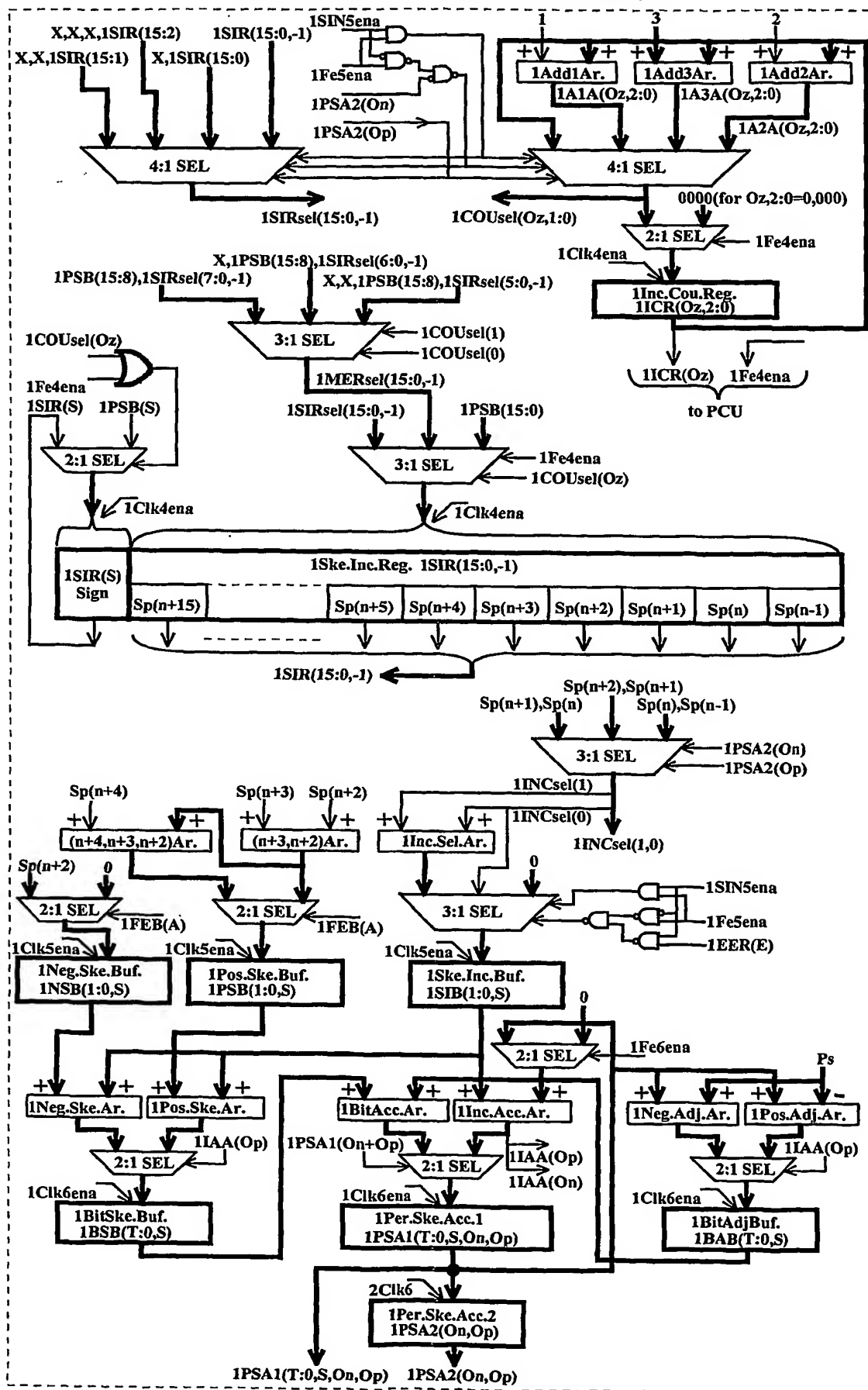


FIG.3B Periodical Skew Accumulation



(DCR(Cf)/DCR(Cs) rising edge writes DCR(7:0)/DCR(15:8) accordingly into PCU Input Register)

(DCR(Cf)/DCR(Cs) rising edge writes DCR(7:0)/DCR(15:8) accordingly into PCU Input Register)

FIG.3D Data Frequency Capturing

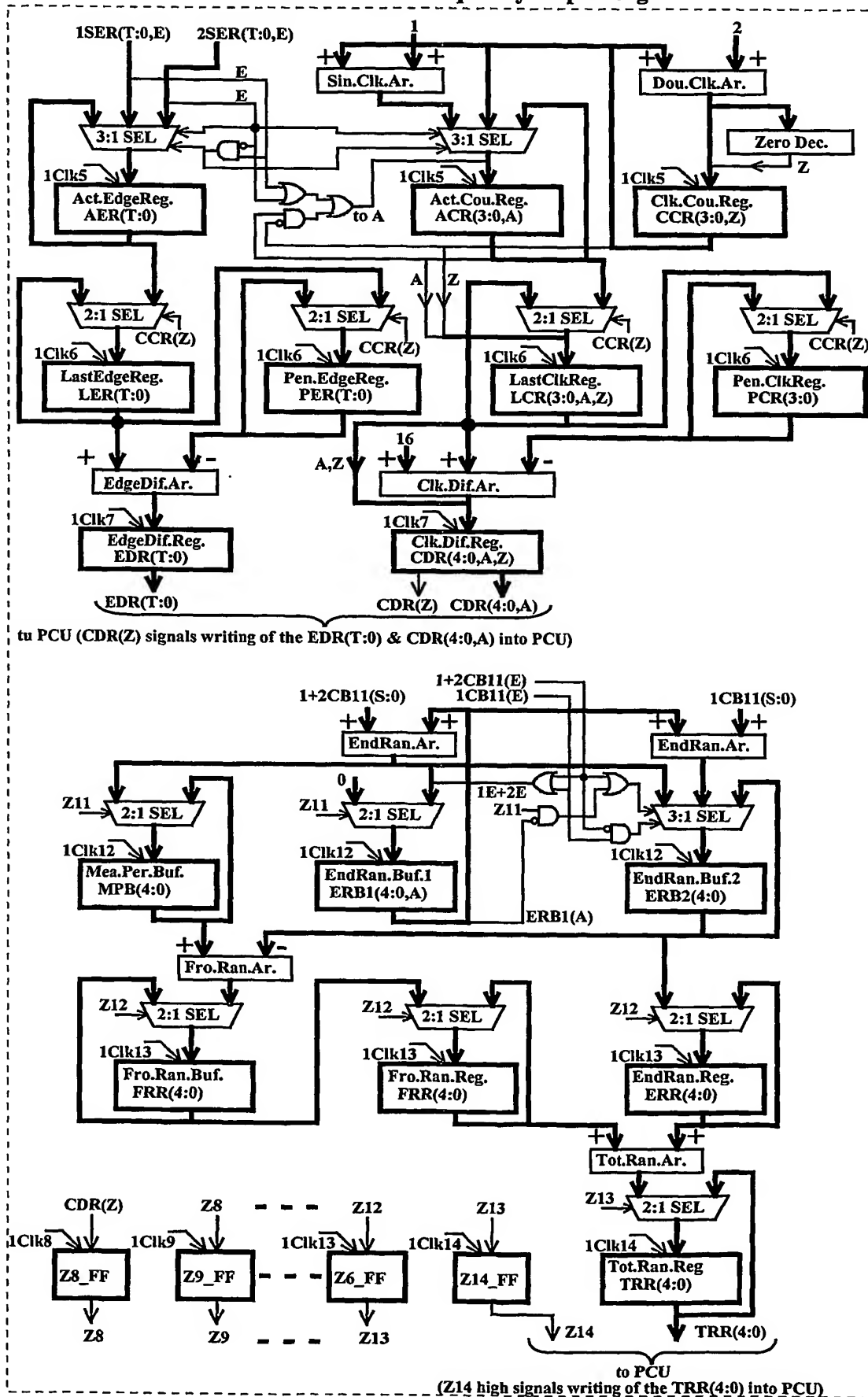


FIG.4A Wave Form Screening & Capturing (WFSC)

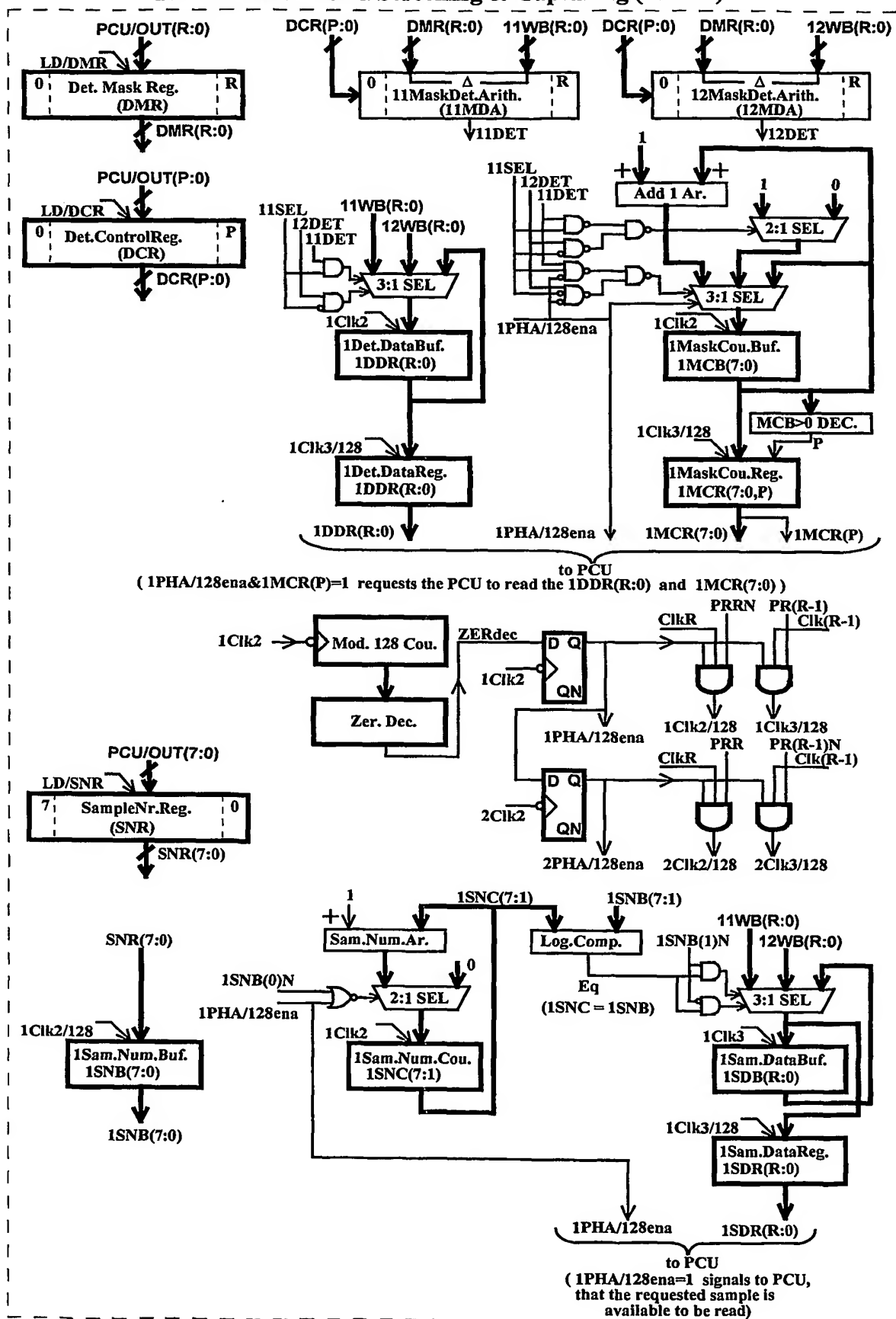
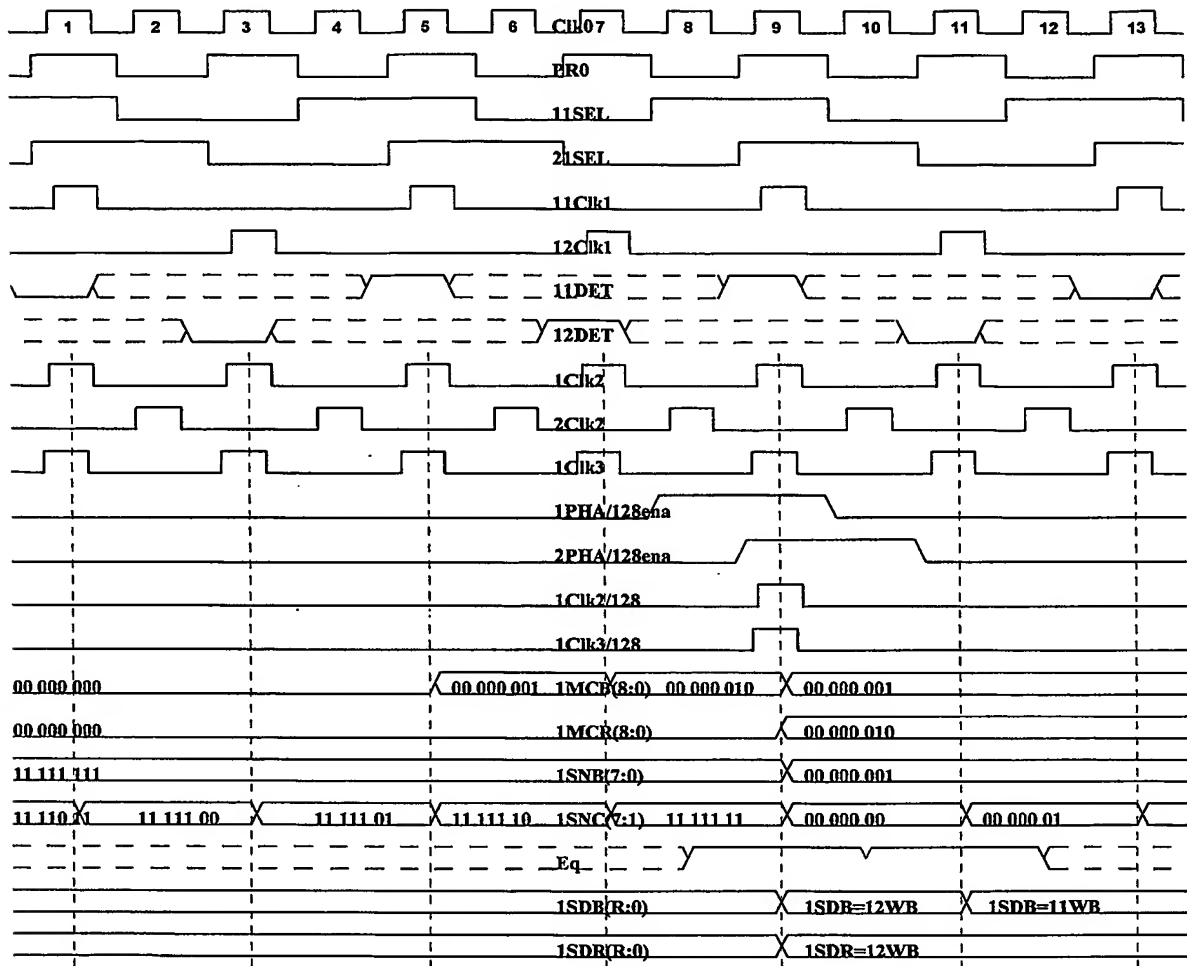


FIG.4B Timing Diagrams of the WFSC



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